UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,367	02/28/2002	Ryota Nanjo	020200	9203

23850 7590 05/22/2003

ARMSTRONG,WESTERMAN & HATTORI, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	8

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,367	NANJO ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on th cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-9 and 13-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/084,367. Currently, claims 1-24 are pending.

Election/Restrictions

2. Applicant's election without traverse of the species of Group IV in Paper No. 7 is acknowledged.[1] Claim1-9, 13-17, and 21-24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Claims 18-20 were previously withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention. Election was made **without** traverse in Paper No. 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. *Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 5,610,088 B1) in view of Kapoor (US 5,780,350 B1) and Wolf (Silicon Processing for the VLSI Era: Vol. 2 – Process Integration).*

---

[1] Only claims 10, 11, and 12 read on the species of Group 4, the embodiment of figs. 5A-5H, wherein the resistor is formed prior to the source/drain regions.

Chang et al. disclose a method of manufacturing a semiconductor device (figs. 2A-2G and accompanying text). The method comprises the following steps substantially as claimed: preparing a semiconductor substrate 100 having first and second regions of a first conductivity type, p-type, defined in a principal surface area of the substrate (fig. 2A);[2] forming at least a first gate electrode 120 in a partial area of the first region (fig. 2A); implanting impurities of a second conductivity type, n-type, opposite to the first conductivity type into a surface layer of the second region to form a first impurity diffusion region, n-well 110 (fig. 2A); forming first spacer film 134 on the side surface of the first gate electrode 120 (fig. 2C); by using the first gate electrode and the first spacer film as a mask, implanting impurities of the second conductivity type into a surface layer of the first region to form second impurity diffusion region, heavily doped source/drain 220 (fig. 2C); removing the first spacer film 134 (fig. 2C); and by using the first gate electrode as a mask, implanting impurities of the second conductivity type into a surface layer in the first region to form a third impurity diffusion region, LDD 222 (fig. 2D).

Chang et al. do not teach executing first, second, and third activation processes following the first, second, and third implanting steps, respectively; or executing each of the first to third activation processes at a temperature at least equal to 750°C.

Wolf discloses a method for forming an n-well in a CMOS integrated circuit (pages 428-431). The method comprises the steps of: implanting n-type impurities into a surface of a semiconductor substrate, and thereafter executing an activation process

[2] See Appendix A.

using a thermal treatment to form the n-well (page 430, fig. 6-35(a) and page 428, par. 5 – page 430, par. 1).[3]

Kapoor discloses a method for forming an integrated circuit (figs. 3-9 and accompanying text). The method comprises the steps of: forming first spacer film 30 on the side surface of a first gate electrode 12 (fig. 3); by using the first gate electrode and the first spacer film as a mask, implanting n-type impurities into a surface layer of a substrate, and thereafter executing an activation process using a thermal treatment to form heavily doped source/drain region 36/38 (fig. 4 and col. 4, lines 54-64);[4] removing the first spacer film 30 (fig. 7); and by using the first gate electrode as a mask, implanting n-type impurities into a surface layer in the substrate, and thereafter executing an activation process at a temperature of 950°C to form LDD 56/58 (fig. 8 and col. 5, lines 49-62).

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to execute first, second, and third activation processes following the first, second, and third implanting steps, respectively, because the n-well 110, heavily doped source/drain 220, and LDD 222 are not formed until the dopant impurities are activated.

4. *Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Kapoor and Wolf as applied to claim 10 above, and further in view of Shibata (US 4,622,735 B1).*

---

[3] Inherently, the activation process is performed at a temperature of at least 750°C because a temperature of at least 750°C is required to activate and diffuse the implanted dopant impurity.
[4] See footnote no. 2.

As discussed above, Chang et al. teach using a first gate electrode as a mask, implanting impurities of the second conductivity type into a surface layer in the first region to form a third impurity diffusion region, LDD 222. Again, Kapoor teaches using a gate electrode as a mask, implanting n-type impurities into a surface layer in the substrate, and thereafter executing an activation process to form LDD 56/58. Neither Chang et al. or Kapoor teach, separately or combined, the limitation of using a laser thermal process for the third activation process.

Shibata discloses a method for forming an integrated circuit (e.g. figs. 1A-1G and accompanying text). The method comprises implanting impurities, and using a laser thermal process for the activation of source/drain regions (col. 3, lines 21-31).

One having ordinary skill in the art would have been motivated to modify the combination of Chang et al., wolf, and Kapoor, at the time the invention was made, by using a thermal process for the third activation process because laser annealing allows the substrate to be heated to a high temperature. Heating the substrate to a high temperature results in excellent crystallinity, as compared to rapid thermal processing. Laser annealing results in source/drain regions with lower resistivity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMJ
May 19, 2003

Mary Wilczewski
Primary Examiner

Appendix A

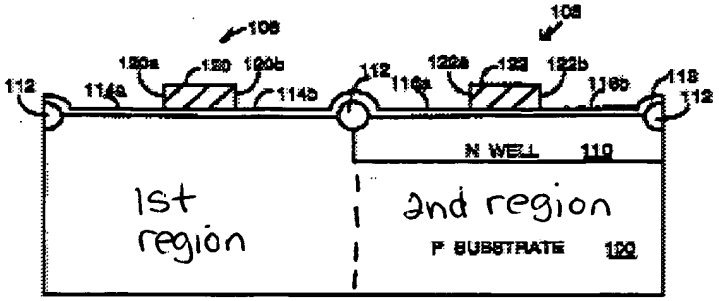

FIG. 2A